MCP3204/3208

2.7V 4-Channel/8-Channel 12-Bit A/D Converters with SPI™

FEATURES

- 12-bit resolution
- ± 1 LSB max DNL
- ± 1 LSB max INL (MCP3204/3208-B)
- ± 2 LSB max INL (MCP3204/3208-C)
- 4 (MCP3204) or 8 (MCP3208) input channels
- Analog inputs programmable as single-ended or pseudo differential pairs
- On-chip sample and hold
- SPI™ serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100ksps max. sampling rate at VDD = 5V
- 50ksps max. sampling rate at VDD = 2.7V
- Low power CMOS technology
  - 500 nA typical standby current, 2µA max.
  - 400 µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- Available in PDIP, SOIC and TSSOP packages

APPLICATIONS

- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

DESCRIPTION

The Microchip Technology Inc. MCP3204/3208 devices are successive approximation 12-bit Analog-to-Digital (A/D) Converters with on-board sample and hold circuitry. The MCP3204 is programmable to provide two pseudo-differential input pairs or four single-ended inputs. The MCP3208 is programmable to provide four pseudo-differential input pairs or eight single-ended inputs. Differential Nonlinearity (DNL) is specified at ±1 LSB, and Integral Nonlinearity (INL) is offered in ±1 LSB (MCP3204/3208-B) and ±2 LSB (MCP3204/3208-C) versions. Communication with the devices is done using a simple serial interface compatible with the SPI protocol. The devices are capable of conversion rates of up to 100ksps. The MCP3204/3208 devices operate over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500nA and 320µA, respectively. The MCP3204 is offered in 14-pin PDIP, 150mil SOIC and TSSOP packages, and the MCP3208 is offered in 16-pin PDIP and SOIC packages.

SPI is a trademark of Motorola Inc.
1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

\[ V_{DD} = \text{+2.7V to 5.5V Power Supply} \]
\[ DGND = \text{Digital Ground} \]
\[ AGND = \text{Analog Ground} \]
\[ CH0-CH7 = \text{Analog Inputs} \]
\[ CLK = \text{Serial Clock} \]
\[ D_{IN} = \text{Serial Data In} \]
\[ D_{OUT} = \text{Serial Data Out} \]
\[ CS/SHDN = \text{Chip Select/Shutdown Input} \]
\[ V_{REF} = \text{Reference Voltage Input} \]

*Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

All parameters apply at \( V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_{AMB} = -40^\circ C \text{ to } +85^\circ C, f_{SAMPLE} = 100\text{ksps} \text{ and } f_{CLK} = 20\times f_{SAMPLE} \), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conversion Time</td>
<td>( t_{CONV} )</td>
<td></td>
<td>12</td>
<td>clock cycles</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Input Sample Time</td>
<td>( t_{SAMPLE} )</td>
<td></td>
<td>1.5</td>
<td>clock cycles</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Throughput Rate</td>
<td>( f_{SAMPLE} )</td>
<td></td>
<td>100</td>
<td>ksp</td>
<td></td>
<td>( V_{DD} = V_{REF} = 5V )</td>
</tr>
<tr>
<td>DC Accuracy</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
<td>bits</td>
<td></td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>( \text{INL} )</td>
<td>( \pm 0.75 )</td>
<td>( \pm 1 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Nonlinearity</td>
<td>( \text{DNL} )</td>
<td>( \pm 0.5 )</td>
<td>( \pm 1 )</td>
<td>No missing codes over temperature</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Error</td>
<td></td>
<td>( \pm 1.25 )</td>
<td>( \pm 3 )</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Error</td>
<td></td>
<td>( \pm 1.25 )</td>
<td>( \pm 5 )</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic Performance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td></td>
<td>-82</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal to Noise and Distortion (SINAD)</td>
<td></td>
<td>72</td>
<td>dB</td>
<td>VIN = 0.1V to 4.9V@1kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spurious Free Dynamic Range</td>
<td></td>
<td>86</td>
<td>dB</td>
<td>VIN = 0.1V to 4.9V@1kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Range</td>
<td></td>
<td>0.25</td>
<td>V</td>
<td>( V_{DD} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Drain</td>
<td></td>
<td>100</td>
<td>150</td>
<td>( \mu A )</td>
<td></td>
<td>( CS = V_{DD} = 5V )</td>
</tr>
<tr>
<td>Analog Inputs</td>
<td></td>
<td>V</td>
<td>V</td>
<td>( V_{SS} )</td>
<td>( V_{REF} )</td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range for CH0-CH7 in Single-Ended Mode</td>
<td>( V_{SS} )</td>
<td>( V_{REF} )</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range for IN+ In pseudo-differential Mode</td>
<td>( \text{IN}^- )</td>
<td>( \text{V}_{\text{REF}+\text{IN}^-} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range for IN- In pseudo-differential Mode</td>
<td>( V_{SS}-100 )</td>
<td>( V_{SS}+100 )</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leakage Current</td>
<td></td>
<td>0.001</td>
<td>±1</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (CONTINUED)

All parameters apply at \( V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_{AMB} = -40^\circ C \) to \( +85^\circ C \), \( f_{SAMPLE} = 100\text{ksps} \) and \( f_{CLK} = 20f_{SAMPLE} \), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch Resistance</td>
<td></td>
<td>1K</td>
<td></td>
<td></td>
<td>Ω</td>
<td>See Figure 4-1</td>
</tr>
<tr>
<td>Sample Capacitor</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>pF</td>
<td>See Figure 4-1</td>
</tr>
</tbody>
</table>

#### Digital Input/Output

- **Data Coding Format**: Straight Binary
- **High Level Input Voltage**: \( V_{IH} \) 0.7 \( V_{DD} \)
- **Low Level Input Voltage**: \( V_{IL} \) 0.3 \( V_{DD} \)
- **High Level Output Voltage**: \( V_{OH} \) 4.1 \( V \)
- **Low Level Output Voltage**: \( V_{OL} \) 0.4 \( V \)
- **Input Leakage Current**: \( I_{LI} \) -10 \( \mu A \)
- **Output Leakage Current**: \( I_{LO} \) -10 \( \mu A \)
- **Pin Capacitance (All Inputs/Outputs)**: \( C_{IN}, C_{OUT} \) 10 \( pF \) \( V_{DD} = 5.0V \) (Note 1) \( T_{AMB} = 25^\circ C, f = 1 \text{ MHz} \)

#### Timing Parameters

- **Clock Frequency**: \( f_{CLK} \) 2.0 \( MHz \) \( f_{CLK} = 2.0 \text{ MHz} \) \( V_{DD} = 5V \) (Note 3) \( V_{DD} = 2.7V \) (Note 3)
- **Clock High Time**: \( t_{HI} \) 250 ns
- **Clock Low Time**: \( t_{LO} \) 250 ns
- **CS Fall To First Rising CLK Edge**: \( t_{SU} \) 100 ns
- **Data Input Setup Time**: \( t_{SU} \) 50 ns
- **Data Input Hold Time**: \( t_{HD} \) 50 ns
- **CLK Fall To Output Data Valid**: \( t_{DO} \) 200 ns See Test Circuits, Figure 1-2
- **CLK Fall To Output Enable**: \( t_{EN} \) 200 ns See Test Circuits, Figure 1-2
- **CS Rise To Output Disable**: \( t_{DIS} \) 100 ns See Test Circuits, Figure 1-2
- **CS Disable Time**: \( t_{CS} \) 500 ns
- **D\text{OUT} Rise Time**: \( t_{R} \) 100 ns See Test Circuits, Figure 1-2 (Note 1)
- **D\text{OUT} Fall Time**: \( t_{F} \) 100 ns See Test Circuits, Figure 1-2 (Note 1)

#### Power Requirements

- **Operating Voltage**: \( V_{DD} \) 2.7 \( V \) \( 5.5 \) \( V \)
- **Operating Current**: \( I_{DD} \) 320 \( \mu A \) \( 400 \) \( \mu A \) \( V_{DD} = V_{REF} = 5V, D_{OUT} \text{ unloaded} \)
- **Standby Current**: \( I_{DDS} \) 2 \( \mu A \) \( CS = V_{DD} = 5.0V \)

**Note 1**: This parameter is guaranteed by characterization and not 100% tested.

**Note 2**: See graphs that relate linearity performance to \( V_{REF} \) levels.

**Note 3**: Because the sample cap will eventually lose charge, effective clock rates below 10kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.
**FIGURE 1-1:** Serial Interface Timing.

- **Waveform 1** is for an output with internal conditions such that the output is high, unless disabled by the output control.
- **Waveform 2** is for an output with internal conditions such that the output is low, unless disabled by the output control.

**FIGURE 1-2:** Test Circuits.

- **Load circuit for** $t_R$, $t_F$, $t_{DO}$
  - $D_{OUT}$
  - $1.4V$
  - $3K$
  - Test Point
  - $C_L = 100pF$

- **Voltage Waveforms for** $t_R$, $t_F$
  - $D_{OUT}$
  - $V_{OH}$
  - $V_{OL}$
  - $t_R$
  - $t_F$

- **Voltage Waveforms for** $t_{DO}$
  - $CLK$
  - $D_{OUT}$
  - $t_{DO}$

- **Load circuit for** $t_{DIS}$ and $t_{EN}$
  - $D_{OUT}$
  - $3K$
  - $V_{DD}/2$
  - $100pF$
  - Test Point

- **Voltage Waveforms for** $t_{DIS}$
  - $D_{OUT}$
  - $D_{OUT}$
  - $CS$
  - $t_{DIS}$

- **Voltage Waveforms for** $t_{EN}$
  - $CS$
  - $CLK$
  - $1$
  - $2$
  - $3$
  - $4$
  - $B11$
  - $V_{SH}$
  - $T_{DIS}$

* Waveform 1 is for an output with internal conditions such that the output is high, unless disabled by the output control.
† Waveform 2 is for an output with internal conditions such that the output is low, unless disabled by the output control.
2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: Unless otherwise indicated, \( V_{DD} = V_{REF} = 5V \), \( V_{SS} = 0V \), \( f_{SAMPLE} = 100k\text{spS} \), \( f_{CLK} = 20 \cdot f_{SAMPLE} \), \( T_A = 25^\circ C \)

**FIGURE 2-1:** Integral Nonlinearity (INL) vs. Sample Rate.

**FIGURE 2-2:** Integral Nonlinearity (INL) vs. \( V_{REF} \).

**FIGURE 2-3:** Integral Nonlinearity (INL) vs. Code (Representative Part).

**FIGURE 2-4:** Integral Nonlinearity (INL) vs. Sample Rate (\( V_{DD} = 2.7V \)).

**FIGURE 2-5:** Integral Nonlinearity (INL) vs. \( V_{REF} \) (\( V_{DD} = 2.7V \)).

**FIGURE 2-6:** Integral Nonlinearity (INL) vs. Code (Representative Part, \( V_{DD} = 2.7V \)).
Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ksps, $f_{CLK} = 20 \times f_{SAMPLE}$, $T_A = 25^\circ C$

FIGURE 2-7: Integral Nonlinearity (INL) vs. Temperature.

FIGURE 2-8: Differential Nonlinearity (DNL) vs. Sample Rate.

FIGURE 2-9: Differential Nonlinearity (DNL) vs. $V_{REF}$.

FIGURE 2-10: Integral Nonlinearity (INL) vs. Temperature ($V_{DD} = 2.7V$).

FIGURE 2-11: Differential Nonlinearity (DNL) vs. Sample Rate ($V_{DD} = 2.7V$).

FIGURE 2-12: Differential Nonlinearity (DNL) vs. $V_{REF}$ ($V_{DD} = 2.7V$).
Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100\text{ksps}$, $f_{CLK} = 20 \times f_{SAMPLE}$, $T_A = 25^\circ\text{C}$

**FIGURE 2-13:** Differential Nonlinearity (DNL) vs. Code (Representative Part).

**FIGURE 2-14:** Differential Nonlinearity (DNL) vs. Temperature.

**FIGURE 2-15:** Gain Error vs. $V_{REF}$.

**FIGURE 2-16:** Differential Nonlinearity (DNL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

**FIGURE 2-17:** Differential Nonlinearity (DNL) vs. Temperature ($V_{DD} = 2.7V$).

**FIGURE 2-18:** Offset Error vs. $V_{REF}$.
Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100ksp$, $f_{CLK} = 20 \times f_{SAMPLE}$, $T_A = 25^\circ C$
Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ksp, $f_{CLK} = 20* f_{SAMPLE}$, $T_A = 25^\circ C$

**FIGURE 2-25:** Effective Number of Bits (ENOB) vs. $V_{REF}$.

**FIGURE 2-26:** Spurious Free Dynamic Range (SFDR) vs. Input Frequency.

**FIGURE 2-27:** Frequency Spectrum of 10kHz input (Representative Part).

**FIGURE 2-28:** Effective Number of Bits (ENOB) vs. Input Frequency.

**FIGURE 2-29:** Power Supply Rejection (PSR) vs. Ripple Frequency.

**FIGURE 2-30:** Frequency Spectrum of 1kHz input (Representative Part, $V_{DD} = 2.7V$).
Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100k$sp, $f_{CLK} = 20^* f_{SAMPLE}$, $T_A = 25^\circ C$
Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100k$sp$s$, $f_{CLK} = 20* f_{SAMPLE}, T_A = 25^\circ C$

FIGURE 2-37: $I_{DDS}$ vs. $V_{DD}$.

FIGURE 2-38: $I_{DDS}$ vs. Temperature.

FIGURE 2-39: Analog Input Leakage Current vs. Temperature.
3.0 PIN DESCRIPTIONS

3.1 CH0 - CH7
Analog inputs for channels 0 - 7 respectively for the multiplexed inputs. Each pair of channels can be programmed to be used as two independent channels in single ended-mode or as a single pseudo-differential input where one channel is IN+ and one channel is IN-. See Section 4.1 and Section 5.0 for information on programming the channel configuration.

3.2 CS/SHDN (Chip Select/Shutdown)
The CS/SHDN pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The CS/SHDN pin must be pulled high between conversions.

3.3 CLK (Serial Clock)
The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed.

3.4 DIN (Serial Data Input)
The SPI port serial data input pin is used to load channel configuration data into the device.

3.5 DOUT (Serial Data output)
The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

3.6 AGND
Analog ground connection to internal analog circuitry.

3.7 DGND
Digital ground connection to internal digital circuitry.

4.0 DEVICE OPERATION
The MCP3204/3208 A/D Converters employ a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the fourth rising edge of the serial clock after the start bit has been received. Following this sample time, the device uses the collected charge on the internal sample and hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100ksps are possible on the MCP3204/3208. See Section 6.2 for information on minimum clock rates. Communication with the device is done using a 4-wire SPI-compatible interface.

4.1 Analog Inputs
The MCP3204/3208 devices offer the choice of using the analog input channels configured as single-ended inputs or pseudo-differential pairs. The MCP3204 can be configured to provide two pseudo-differential input pairs or four single-ended inputs. The MCP3208 can be configured to provide four pseudo-differential input pairs or eight single-ended inputs. Configuration is done as part of the serial command before each conversion begins. When used in the pseudo-differential mode, each channel pair (i.e., CH0 and CH1, CH2 and CH3 etc.) are programmed as the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to (VREF + IN-). The IN- input is limited to ±100mV from the VSS rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than [(VREF + (IN-)) - 1 LSB], then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below Vss, then the voltage level at the IN+ input will have to go below Vss to see the 000h output code. Conversely, if IN- is more than 1 LSB above VSS, then the FFFh code will not be seen unless the IN+ input level goes above VREF level.

For the A/D Converter to meet specification, the charge holding capacitor, CSAMPLE must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram it is shown that the source impedance (RS) adds to the internal sampling switch (Rss) impedance, directly affecting the time that is required to charge the capacitor, CSAMPLE. Consequently, larger source impedances increase the offset, gain, and integral linearity errors of the conversion. See Figure 4-2.

4.2 Reference Input
For each device in the family, the reference input (VREF) determines the analog input voltage range. As the reference input is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is a function of the analog input signal and the reference input as shown below.

\[ \text{Digital Output Code} = \frac{4096 \times V_{IN}}{V_{REF}} \]

where:

\[ V_{IN} = \text{analog input voltage} \]
\[ V_{REF} = \text{reference voltage} \]

When using an external voltage reference device, the system designer should always refer to the manufacturer’s recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the A/D Converter.
FIGURE 4-1: Analog Input Model

Legend
- VA = Signal Source
- Rs = Source Impedance
- CHx = Input Channel Pad
- C_PIN = Input Capacitance
- VT = Threshold Voltage
- I_LEAKAGE = Leakage Current at the pin due to various junctions
- SS = Sampling Switch
- RSS = Sampling Switch Resistor
- CSAMPLE = Sample/Hold Capacitance

FIGURE 4-2: Maximum Clock Frequency vs. Input resistance (Rs) to maintain less than a 0.1LSB deviation in INL from nominal conditions.
5.0 SERIAL COMMUNICATIONS

Communication with the MCP3204/3208 devices is done using a standard SPI-compatible serial interface. Initiating communication with either device is done by bringing the CS line low. See Figure 5-1. If the device was powered up with the CS pin low, it must be brought high and back low to initiate communication. The first clock received with CS low and D\textsubscript{IN} high will constitute a start bit. The SGL/DIFF bit follows the start bit and will determine if the conversion will be done using single ended or differential input mode. The next three bits (D0, D1 and D2) are used to select the input channel configuration. Table 5-1 and Table 5-2 show the configuration bits for the MCP3204 and MCP3208, respectively. The device will begin to sample the analog input on the fourth rising edge of the clock after the start bit has been received. The sample period will end on the falling edge of the fifth clock following the start bit.

After the D0 bit is input, one more clock is required to complete the sample and hold period (D\textsubscript{IN} is a don't care for this clock). On the falling edge of the next clock, the device will output a low null bit. The next 12 clocks will output the result of the conversion with MSB first as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the CS is held low, the device will output the conversion result LSB first as shown in Figure 5-2. If more clocks are provided to the device while CS is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring CS low and clock in leading zeros on the D\textsubscript{IN} line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 for more details on using the MCP3204/3208 devices with hardware SPI ports.

<table>
<thead>
<tr>
<th>CONTROL BIT SELECTIONS</th>
<th>INPUT CONFIGURATION</th>
<th>CHANNEL SELECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINGLE/DIFF D2 D1 D0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 X 0 0 0</td>
<td>single ended</td>
<td>CH0</td>
</tr>
<tr>
<td>1 X 0 0 1</td>
<td>single ended</td>
<td>CH1</td>
</tr>
<tr>
<td>1 X 1 0 0</td>
<td>single ended</td>
<td>CH2</td>
</tr>
<tr>
<td>1 X 1 1 0</td>
<td>single ended</td>
<td>CH3</td>
</tr>
<tr>
<td>0 X 0 0 0</td>
<td>differential</td>
<td>CH0 = IN- CH1 = IN-</td>
</tr>
<tr>
<td>0 X 0 0 1</td>
<td>differential</td>
<td>CH0 = IN- CH1 = IN+</td>
</tr>
<tr>
<td>0 X 1 0 0</td>
<td>differential</td>
<td>CH2 = IN+ CH3 = IN+</td>
</tr>
<tr>
<td>0 X 1 0 1</td>
<td>differential</td>
<td>CH2 = IN+ CH3 = IN-</td>
</tr>
<tr>
<td>0 X 1 1 0</td>
<td>differential</td>
<td>CH6 = IN- CH7 = IN-</td>
</tr>
<tr>
<td>0 X 1 1 1</td>
<td>differential</td>
<td>CH6 = IN+ CH7 = IN+</td>
</tr>
</tbody>
</table>

*D2 is don’t care for MCP3204

**TABLE 5-1:** Configuration Bits for the MCP3204.

<table>
<thead>
<tr>
<th>CONTROL BIT SELECTIONS</th>
<th>INPUT CONFIGURATION</th>
<th>CHANNEL SELECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINGLE/DIFF D2 D1 D0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 X 0 0 0</td>
<td>single ended</td>
<td>CH0</td>
</tr>
<tr>
<td>1 X 0 0 1</td>
<td>single ended</td>
<td>CH1</td>
</tr>
<tr>
<td>1 X 1 0 0</td>
<td>single ended</td>
<td>CH2</td>
</tr>
<tr>
<td>1 X 1 1 0</td>
<td>single ended</td>
<td>CH3</td>
</tr>
<tr>
<td>0 X 0 0 0</td>
<td>differential</td>
<td>CH0 = IN+ CH1 = IN-</td>
</tr>
<tr>
<td>0 X 0 0 1</td>
<td>differential</td>
<td>CH0 = IN+ CH1 = IN-</td>
</tr>
<tr>
<td>0 X 1 0 0</td>
<td>differential</td>
<td>CH2 = IN+ CH3 = IN-</td>
</tr>
<tr>
<td>0 X 1 0 1</td>
<td>differential</td>
<td>CH2 = IN+ CH3 = IN+</td>
</tr>
<tr>
<td>0 X 1 1 0</td>
<td>differential</td>
<td>CH6 = IN- CH7 = IN-</td>
</tr>
<tr>
<td>0 X 1 1 1</td>
<td>differential</td>
<td>CH6 = IN+ CH7 = IN-</td>
</tr>
</tbody>
</table>

**TABLE 5-2:** Configuration Bits for the MCP3208.
FIGURE 5-1: Communication with the MCP3204 or MCP3208.

* After completing the data transfer, if further clocks are applied with CS low, the A/D Converter will output LSB first data, then followed with zeros indefinitely. See Figure 5-2 below.

** tDATA: during this time, the bias current and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-2: Communication with MCP3204 or MCP3208 in LSB First Format.

* After completing the data transfer, if further clocks are applied with CS low, the A/D Converter will output zeros indefinitely.

** tDATA: During this time, the bias circuit and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out LSB first data or zeroes.
6.0 APPLICATIONS INFORMATION

6.1 Using the MCP3204/3208 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Because communication with the MCP3204/3208 devices may not need multiples of eight clocks, it will be necessary to provide more clocks than are required. This is usually done by sending 'leading zeros' before the start bit. As an example, Figure 6-1 and Figure 6-2 shows how the MCP3204/3208 can be interfaced to a MCU with a hardware SPI port. Figure 6-1 depicts the operation shown in SPI Mode 0,0 which requires that the SCLK from the MCU idles in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1 where the clock idles in the 'high' state.

As shown in Figure 6-1, the first byte transmitted to the A/D Converter contains five leading zeros before the start bit. Arranging the leading zeros this way produces the output 12 bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D Converter on the falling edge of clock number 12. After the second eight clocks have been sent to the device, the MCUs receive buffer will contain three unknown bits (the output is at high impedance for the first two clocks), the null bit and the highest order four bits of the conversion. After the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Easier manipulation of the converted data can be obtained by using this method.

Figure 6-2 shows the same thing in SPI Mode 1,1 which requires that the clock idles in the high state. As with mode 0,0, the A/D Converter outputs data on the falling edge of the clock and the MCU latches data from the A/D Converter in on the rising edge of the clock.

FIGURE 6-1: SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).

FIGURE 6-2: SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).
6.2 Maintaining Minimum Clock Speed

When the MCP3204/3208 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample capacitor while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2ms (effective clock frequency of 10kHz). Failure to meet this criterion may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D Converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D Converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur. See Figure 4-2. It is also recommended that a filter be used to eliminate any signals that may be aliased back in to the conversion results. This is illustrated in Figure 6-3 where an op amp is used to drive the analog input of the MCP3204/3208. This amplifier provides a low impedance source for the converter input and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip’s free interactive FilterLab™ software. FilterLab will calculate capacitor and resistors values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 “Anti-Aliasing Analog Filters for Data Acquisition Systems.”

6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing $V_{DD}$ connections to devices in a “star” configuration can also reduce noise by eliminating return current paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D Converters, refer to AN688 “Layout Tips for 12-Bit A/D Converter Applications.”

**FIGURE 6-3:** The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3204.

**FIGURE 6-4:** $V_{DD}$ traces arranged in a ‘Star’ configuration in order to reduce errors caused by current return paths.

FilterLab is a trademark of Microchip Technology Inc. in the U.S.A and other countries. All rights reserved.
6.5 Utilizing the Digital and Analog Ground Pins

The MCP3204/3208 devices provide both digital and analog ground connections to provide another means of noise reduction. As shown in Figure 6-5, the analog and digital circuitry is separated internal to the device. This reduces noise from the digital portion of the device being coupled into the analog portion of the device. The two grounds are connected internally through the substrate which has a resistance of 5 - 10 Ω.

If no ground plane is utilized, then both grounds must be connected to VSS on the board. If a ground plane is available, both digital and analog ground pins should be connected to the analog ground plane. If both an analog and a digital ground plane are available, both the digital and the analog ground pins should be connected to the analog ground plane. Following these steps will reduce the amount of digital noise from the rest of the board being coupled into the A/D Converter.

---

**FIGURE 6-5:** Separation of Analog and Digital Ground Pins.
MCP3204 PRODUCT IDENTIFICATION SYSTEMS

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>MCP3204   - G T /P</th>
</tr>
</thead>
</table>
| Package:  P = PDIP (14 lead)  
SL = SOIC (150 mil Body), 14 lead  
ST = TSSOP, 14 lead (C Grade only) |
| Temperature Range:  I = –40°C to +85°C |
| Performance Grade:  B = ±1 LSB INL (TSSOP not available in this grade)  
C = ±2 LSB INL |
| Device:  MCP3204 = 4-Channel 12-Bit Serial A/D Converter  
MCP3204T = 4-Channel 12-Bit Serial A/D Converter on tape and reel (SOIC and TSSOP packages only) |

MCP3208 PRODUCT IDENTIFICATION SYSTEMS

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>MCP3208   - G T /P</th>
</tr>
</thead>
</table>
| Package:  P = PDIP (16 lead)  
SL = SOIC (150 mil Body), 16 lead |
| Temperature Range:  I = –40°C to +85°C |
| Performance Grade:  B = ±1 LSB INL (TSSOP not available in this grade)  
C = ±2 LSB INL |
| Device:  MCP3208 = 8-Channel 12-Bit Serial A/D Converter  
MCP3208T = 8-Channel 12-Bit Serial A/D Converter on tape and reel (SOIC packages only) |

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.
WORLDWIDE SALES AND SERVICE

AMERICAS
Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 2008
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Austin
Analog Product Sales
8803 MoPac Expressway North
Suite A-201
Austin, TX 78759
Tel: 512-345-2030 Fax: 512-345-6085

Boston
Analog Product Sales
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
393 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton
Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1899 Fax: 949-263-1338

Mountain View
Analog Product Sales
1300 Terra Bella Avenue
Mountain View, CA 94043-1836
Tel: 650-967-8241 Fax: 650-967-1590

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-0699

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9866-6733 Fax: 61-2-9866-6755

China - Beijing
Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai
Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xia Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong
Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology India
India Liaison Office
Dyvasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaunessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Int'L Inc.
Soshisei Building
3-18-20, Shinjyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

ASIA/PACIFIC (continued)

Korea
Microchip Technology Korea
168-1, Yongbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 189980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Denmark ApS
Regus Business Centre
Lautrup høj 1-3
Ballerpark DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Greece
Analog Product Sales
Lochhaer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895550-0 Fax: 49-89-895650-22

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Tauris 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winneshields Triangle
Wokingham
Berkshire, England RG41 STU
Tel: 44 118 921-5869 Fax: 44-118 921-5820
01/30/01

All rights reserved. © 2001 Microchip Technology Incorporated. Printed in the USA. 01/30/01 Printed on recycled paper.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, except as maybe explicitly expressed herein, under any intellectual property rights.